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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,347	03/31/2004	Mahesh U. Wagh	42P18578	8283

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 OAKMEAD PARKWAY
SUNNYVALE, CA 94085-4040

EXAMINER	
FRANKLIN, RICHARD B	
ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/815,347	WAGH ET AL.	
	Examiner	Art Unit	
	Richard Franklin	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *1-7 and 20-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-19 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 27 are pending. Claims 1 – 7 and 20 – 24 are withdrawn from consideration.

Response to Arguments

2. Applicant's arguments filed 06 June 2007 have been fully considered but they are not persuasive.

With regards to claims 8 and 25, Applicant has argued that the relied upon references do not teach applicants claimed invention. Specifically, Applicant states that neither US Patent No. 6,240,095 (hereinafter Good) or US Patent No. 5,787,072 (hereinafter Shimojo) do not teach a chipset in the same device as the IO controller. However, the Examiner respectfully disagrees. Applicant states that Good teaches that the remote network device is located in a separate remote server away from the network interface card. However, this is not the case. However, Good is merely giving an example of a network device when stating at the network device can be a remote server. Good states that modifications and variations of the preferred embodiment are still within the scope of the invention (Good; Col 6 Lines 45 – 49), meaning the example given is not limiting. Nowhere does Good teach the network device being away from the network interface card as suggested by applicant. As applicant has not defined the term "device," the Examiner has given the term its broadest reasonable interpretation. Using this interpretation, the whole system of Good can be considered a device.

Therefore, the chipset (Good; Figure 1 Item 12) and the I/O controller (Good; Figure 1 Item 10) are in the same device.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 8 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,240,095 (hereinafter Good) in view of US Patent No. 5,787,072 (hereinafter Shimojo).

As per claims 8 and 25, Good teaches determining an amount of available memory credits in an IO controller (Good; Figure 1 Item 10, Col 5 Lines 24 – 31); communicating to a chipset (Good; Figure 1 Item 12) within a device (See "Response to Arguments" above) coupled to the IO controller within the device (See "Response to Arguments" above) the amount of available memory credits (Good; Col 5 Lines 24 – 31); and sending an amount of data from the chipset to the IO controller (Good; Col 5 Lines 35 – 38).

Good does not explicitly teach that the amount of data sent is one of equivalent to or less than the communicated memory credit amount.

However, Shimojo teaches sending credit amounts (Shimojo; Col 6 Line 61 – Col 7 Line 4) from a receiver to a sender and sending data from the sender to the receiver

(Shimojo; Col 6 Line 61 – Col 7 Line 4), wherein the data is equal to or less than the communicated credit amounts (Shimojo; Col 6 Line 61 – Col 7 Line 4).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Good to include the data size restriction because doing so allows for protection that the cell does not exceed the amount of free buffer area (Shimojo; Col 6 Line 61 – Col 7 Line 4).

4. Claims 9, 12 – 16, 18 – 19, and 26 – 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,240,095 (hereinafter Good) in view of US Patent No. 5,787,072 (hereinafter Shimojo) and further in view of US Patent Application Publication No. 2002/0150049 (hereinafter Collier).

As per claims 9 and 26, Good in combination with Shimojo teach the method as described per claims 8 and 25 (see rejection of claims 8 and 25 above). Good in combination with Shimojo also teaches determining a least amount of available memory in one of the buffers to create an amount of available memory in the IO controller (Good; Col 5 Lines 24 – 31).

Good in combination with Shimojo does not teach wherein determining the available amount of memory credits comprises comparing an amount of available memory in each of a plurality of buffers contained within the IO controller.

However, Collier teaches determining the available amount of memory credits comprises comparing an amount of available memory in each of a plurality of buffers (Collier; Paragraph [0024] Lines 9 – 15 "virtual lane buffers").

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Good in combination with Shimojo to include the comparison because doing so allows for indication that free space has increased over a threshold (Collier; Paragraph [0024]).

As per claims 12 and 13, Good also teaches temporarily storing the data sent from the chipset in a buffer in the IO controller (Good; Col 5 Lines 21 – 61).

As per claim 14, Collier teaches storing the data in a plurality of buffers (Collier; Figure 3 Item 322, Paragraph [0030] Lines 4 – 7, Paragraph [0033] lines 1 – 7).

As per claim 15, Good also teaches emptying the buffer of at least some of the data temporarily stored in the IO controller to create a new amount of available memory credits in the IO controller (Good; Col 6 Lines10 – 14).

As per claim 16, Good also teaches sending the data to an IO bus coupled to the IO controller (Good; Figure 1 Item 18).

As per claim 17, Collier also teaches sending the data to a plurality of IO busses (Infiniband) coupled to the IO controller (Collier; Figure 1, Paragraphs [0018] – [0019]).

As per claim 18, Good also teaches keeping track of the number of available memory credits in the IO controller (Good; Figure 1 Item 74).

As per claim 19, Good also teaches simultaneously keeping track of amounts of memory credits the IO controller empties onto the IO bus (Good; Col 6 Lines 10 – 14), amounts of memory credits sent to the IO controller (Good; Figure 3 Item 60, Col 5 Line 66 – Col 6 Line 4) and amounts of memory credits made available by the distribution of data sent from the chipset to a plurality of buffers contained in the IO controller (Good; Figure 1 Item 74, Col 5 Lines 30 – 32).

As per claim 27, Good also teaches temporarily storing the data sent from the chipset in a buffer in the IO controller (Good; Col 5 Lines 21 – 61); emptying the buffer of at least some of the data temporarily stored in the IO controller to create a new amount of available memory credits in the IO controller (Good; Col 6 Lines10 – 14); and simultaneously keeping track of amounts of memory credits the IO controller empties onto the IO bus (Good; Col 6 Lines 10 – 14), amounts of memory credits sent to the IO controller (Good; Figure 3 Item 60, Col 5 Line 66 – Col 6 Line 4) and amounts of memory credits made available by the distribution of data sent from the chipset to a plurality of buffers contained in the IO controller (Good; Figure 1 Item 74, Col 5 Lines 30 – 32).

5. Claims 10 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,240,095 (hereinafter Good) in view of US Patent No. 5,787,072 (hereinafter Shimojo) further in view of US Patent Application Publication No. 2002/0150049 (hereinafter Collier) and further in view of US Patent Application Publication No. 2003/0223369 (hereinafter Anderson).

As per claims 10 – 11, Good in combination with Shimojo and Collier teach the method as per claim 9 (see rejection of claim 9 above).

Good in combination with Shimojo and Collier does not teach converting the amount of available memory to an amount of available credits by dividing the available memory by the amount of memory equal to one credit.

However, Anderson teaches converting from memory to credits by determining the equivalent credit value of a packet (Anderson; Paragraphs [0039] and [0053]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the teachings of Good in combination with Shimojo and Collier to include the conversion because doing so allows for size comparisons (Anderson; Paragraph [0053]).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Franklin whose telephone number is (571) 272-0669. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Richard Franklin
Patent Examiner
Art Unit 2181

ALFORD KINDRED
PRIMARY EXAMINER